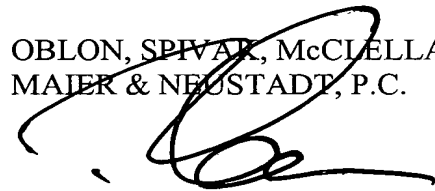## REMARKS

Claims 1-35 are active.

The specification at page 7, line 9, is amended to change the citation of Japanese Laid-open Patent Publication --- 2000-75575 --- to ---2000-75572 ---. JP 2000-75575, was cited in error in the specification. JP2000-75575 is directed to an image forming device where image forming with excessive density and surface staining are reduced, by a developer stirring process executed by a CPU (see attached abstract of JP2000-75575), while a constant current control method is disclosed in the specification at page 7, line 7, through page 8, line 1 and in JP 2000-75572. A copy of the correct reference, JP2000-75572, with the English Abstract is attached herewith for the Examiner's convenience. Accordingly, no new matter would be added by the above amendment. The application is now in condition for examination on its merits. Early examination is respectfully requested.

Respectfully submitted,

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PATENT ABSTRACTS OF JAPAN

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(72)Inventor :   SAITO HIROSHI
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SUGIYAMA TOSHIHIRO

(54) IMAGE FORMING DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide an image forming device where image forming with excessive density and surface staining are surely reduced.
SOLUTION: A CPU firstly executes developer stirring processing for 30 seconds (substep sb1-2) after starting the rotation of a photoreceptive drum (substep sb1-1). The triboelecltricfication of two-component developer is accelerated by the developer stirring processing, so that the surface staining at the non- image part of the photoreceptive drum is reduced. Next, after a P-pattern is formed at a specified position on the photoreceptive drum by the CPU (substep sb1-3), the toner stuck amount measured value (hereinafter referred to as Vsp) of the P-pattern is referred to (substep sb1-4). Then, in the case of judging as Vsp<0.39 (yes at substep sb1-4), it is judged that the surface staining of a quantity exceeding a tolerance is caused on the photoreceptive drum, so that the sequence of control is looped with the substep sb1-2 so as to stir the two-component developer at the inside of a developing device more. Looping is executed until the CPU judges as Vsp≥0.39 at the substep sb1-4.

Sb1 スタート

ドラム回転開始 — Sb1-1

撹拌 — Sb1-2

Pパターン 形成 — Sb1-3

Vsp<0.39 ? — Sb1-4 Y N

ドラム回転終了 — Sb1-5

Sb1 エンド
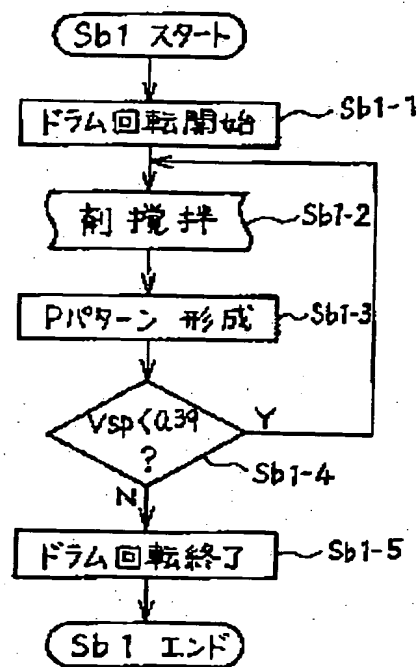
LEGAL STATUS

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